SILICON SENSING®

MEMS Foundry Design Rules

To be the leading provider of affordable, high performance, high integrity MEMS inertial products and foundry services

Possible area for alignment mark

8 inch
6 inch
5 inch
4 inch
96mm
40mm
50mm
13mm
18mm
30mm
174mm

Black; for 4,5,6 inch
Red; for 8 inch

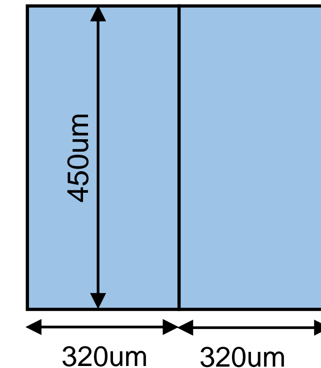
Alignment marks must be placed with the rectangular areas

Alignment accuracy

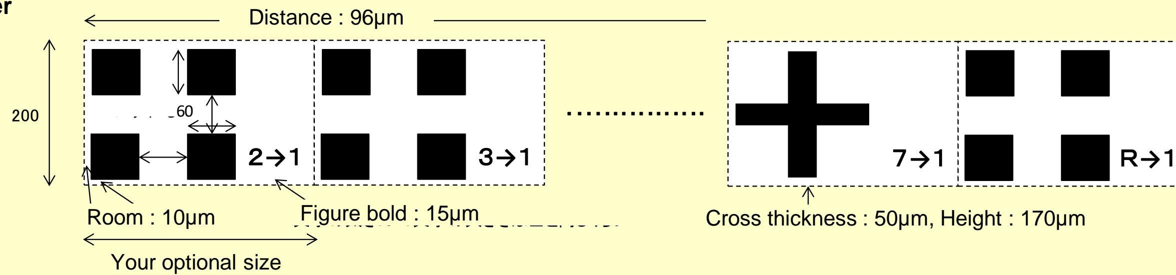
- Both side alignment +/- 5µm
- Top side accuracy +/- 5µm

Field size

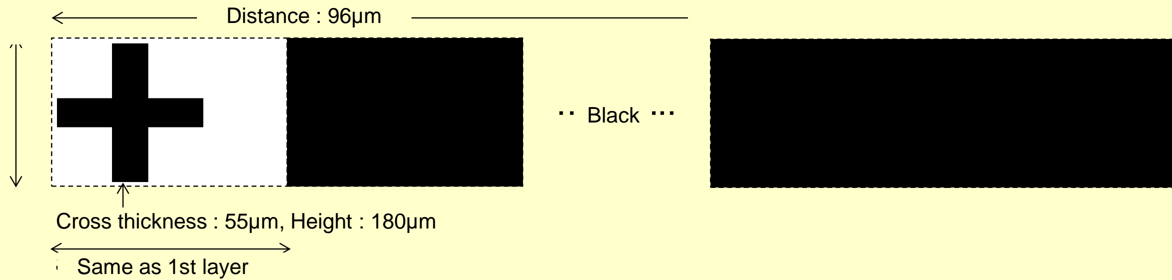
- The size of alignment marks must be within the rectangular area



Example for alignment mark



Second layer



Subsequent layers (example hole-making patterns)

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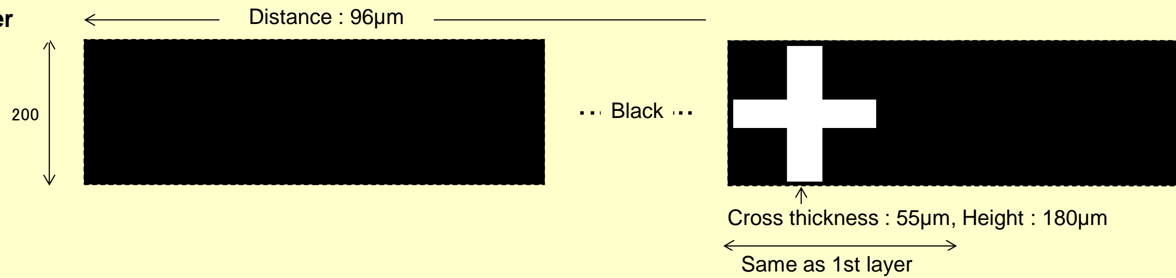
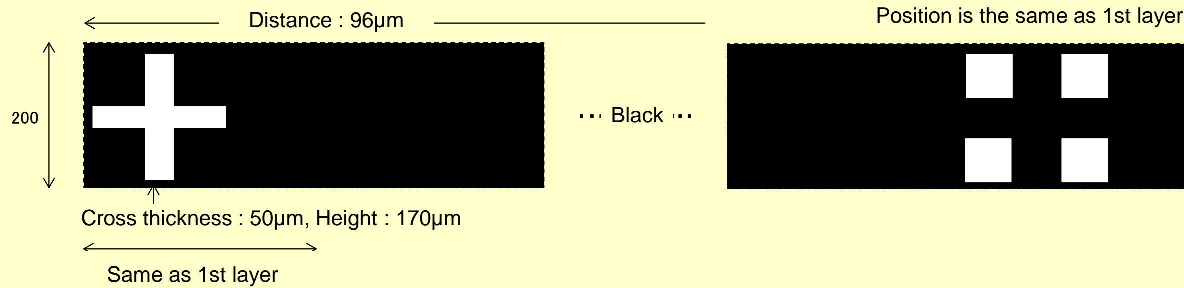


Back side alignment mark



Alignment mark for back side Deep RIE

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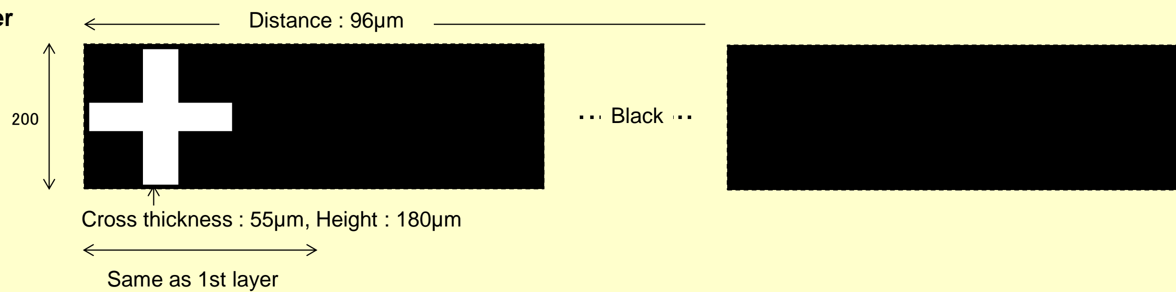

Minimum dimension

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Process	Pattern	Minimum	Note
Si Deep RIE	Slit CD	2.0μm	Maximum aspect ratio is 30 and larger ratios need to be confirmed.
	Slit CD on SOI active layer	3.0μm	Maximum aspect ratio is 30 and larger ratios need to be confirmed.
	Trench CD on SOI active layer	3.0μm	Maximum aspect ratio is 30 and larger ratios need to be confirmed.
	Hole	Φ5.0μm	Maximum aspect ratio is 30 and larger ratios need to be confirmed.
	Pillar	Φ2.0μm	Maximum aspect ratio is 30 and larger ratios need to be confirmed.
	Maximum aspect ratio	100	L/S condition needs to be confirmed.
	Angle	88～92deg	
	Taper	Approx. 75deg	

Uniformity through the wafer depends on the pattern.

Minimum dimension

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Process	Pattern	Minimum	Note
PZT etching	Top electrode on PZT	3.0μm	In the case of PZT thickness 3.0μm
	PZT top edge – top electrode	5.0μm	
	PZT bottom edge – bottom electrode	3.0μm	
SiO2 etching	L/S	2.0μm	
	Hole	Φ3.0μm	
Metal (Milling)	Line CD	3μm	The metal pattern must be away from PZT structure with 3x distance of PZT thickness if the metal pattern is close to the PZT structure.

Design rule using a stepper

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Process	Pattern	Minimum	Note
Exposure with Stepper M1500 UTS	Shot size	･38mm×11.4mm ･30mm×15mm ･21mm×17.5mm	Without alignment mark Alignment mark must be located in this area when necessary.
	L/S	1.0μm	In the case of photoresist thickness 1.0μm
	Wafer size	6 and 8 inch	
	Photomask	5”×5”×0.09”	- Two reticle alignment mark is necessary on the edge. - Mirror-reversed image

Accuracy assurance rule

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Process	Pattern	Minimum	Note
Thin metal film	Uniformity In-house : Al, Au, Cr, Ti, Pt Subcontractor : others	+/-5% Not guaranteed	
Oxidation	Uniformity for thermal or sputter	 +/-5% +/-5%	 Max 3μm Max 1μm
PZT	Uniformity	+/-5%	Max 5um
Si Deep RIE	Depth through the wafer Slit Pillar	+/-5% +/-0.5μm +/-0.5μm	Depends on recipe +/-0.1 is possible. +/-0.1 is possible.
Metal etching (Milling)	Minimum metal line CD	3μm	The metal pattern must be away from PZT structure with 3x distance of PZT thickness if the metal pattern is closed to PZT structure.

PZT electrode etching rule

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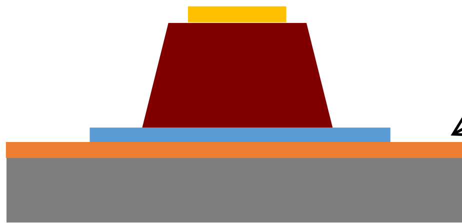
Minimum 0.5µm SiO_2 is necessary for Pt or Au etching as insulation layer.



Edge exclusion for SOI

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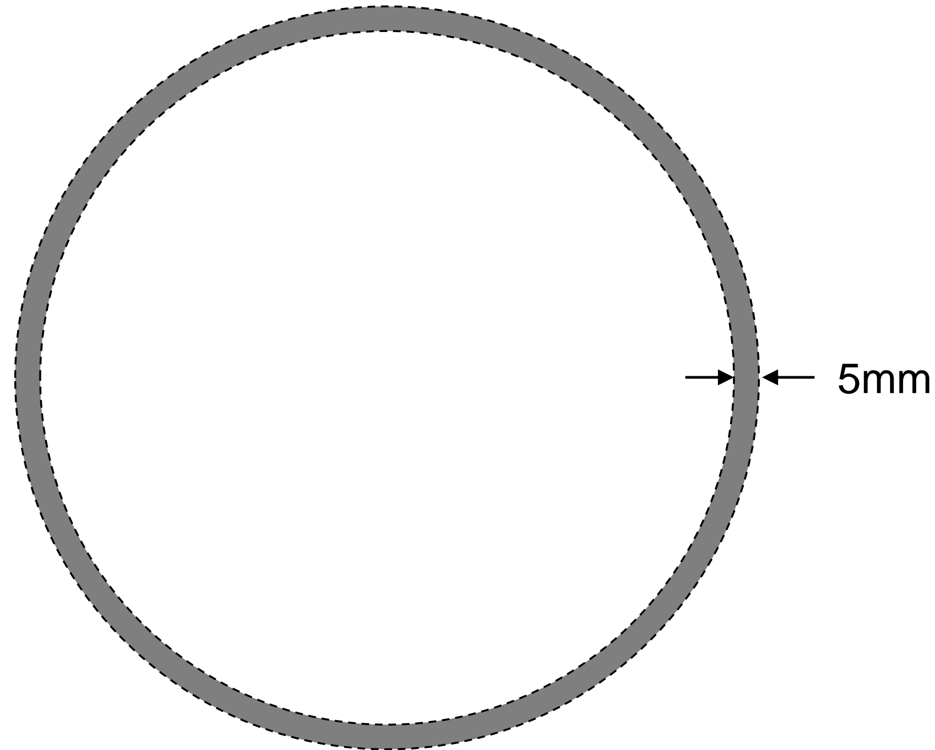

5mm black pattern from the edge is necessary to etch both sides of SOI wafer for all photomasks.

For all enquiries,
contact sales@siliconsensing.com